US009679901B1

(12) **United States Patent**
Wang et al.

(10) **Patent No.: US 9,679,901 B1**
(45) **Date of Patent: Jun. 13, 2017**

(54) **SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF**

(71) Applicants: **United Microelectronics Corp.**, Hsinchu (TW); **Fujian Jinhua Integrated Circuit Co., Ltd.**, Fujian (CN)

(72) Inventors: **Ying-Chiao Wang**, Changua County (TW); **Chien-Ting Ho**, Taichung (TW); **Le-Tien Jung**, Hsinchu (TW); **Shih-Fang Tzou**, Tainan (TW); **Chin-Lung Lin**, Hsinchu (TW); **Harn-Jiunn Wang**, Kaohsiung (TW)

(73) Assignees: **United Microelectronics Corp.**, Hsinchu (TW); **Fujian Jinhua Integrated Circuit Co., Ltd.**, Fujian Province (CN)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **15/296,955**

(22) Filed: **Oct. 18, 2016**

(30) **Foreign Application Priority Data**

Sep. 22, 2016 (CN) 2016 1 0839780

(51) **Int. Cl.**

H01L 21/762	(2006.01)
H01L 27/108	(2006.01)
H01L 29/06	(2006.01)
H01L 21/461	(2006.01)

(52) **U.S. Cl.**
CPC ***H01L 27/10894*** (2013.01); ***H01L 21/461*** (2013.01); ***H01L 21/76224*** (2013.01); ***H01L 27/10897*** (2013.01); ***H01L 29/0649*** (2013.01)

(58) **Field of Classification Search**
CPC . H01L 21/042; H01L 21/0425; H01L 21/048; H01L 21/46; H01L 21/461; H01L 21/64; H01L 21/70; H01L 21/702; H01L 21/71; H01L 21/7602
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,492,073	B1	12/2002	Lin et al.
7,691,549	B1	4/2010	Glasser
7,927,782	B2	4/2011	Aton
8,765,362	B2	7/2014	Oori
9,184,169	B2	11/2015	Kim et al.
9,337,199	B2	5/2016	Kim et al.
2015/0255299	A1	9/2015	Cantone et al.

Primary Examiner — Cheung Lee
(74) *Attorney, Agent, or Firm* — J.C. Patents

(57) **ABSTRACT**

A semiconductor device and a manufacturing method thereof are provided. The semiconductor device includes a substrate, a plurality of active areas, and an isolation structure. The substrate has a device region and a peripheral region surrounding the device region. The active areas are located in the substrate in the device region. When viewed from above, the edges of the ends of the active areas adjacent to the boundary of the device region are aligned with each other, and the width of the ends of the active areas adjacent to the boundary of the device region is greater than the width of the other portions of the active areas. The isolation structure is disposed in the substrate and surrounds the active areas and is located in the peripheral region.

10 Claims, 3 Drawing Sheets